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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,043	12/11/2003	Dietrich Bonart	2000 P 23706 US	8428

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SLATER & MATSIL LLP
17950 PRESTON ROAD
SUITE 1000
DALLAS, TX 75252

EXAMINER	
TRAN, MAI HUONG C	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 06/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/733,043	BONART, DIETRICH	
	Examiner	Art Unit	
	Mai-Huong Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) *18-23* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/29/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restriction

Application's election without traverse of Group I (Claims 1-17) drawn to a semiconductor device is acknowledged for prosecution in the subject application. Accordingly, claims 18-23 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Applicants have the right to file a divisional application covering the subject matter of the non-elected claims.

Drawings

The drawings are objected to for the following reasons.

Figures 4A, 4B, 5A, 5B are not designated by a legend such as "Prior Art". The Legend is necessary in order to clarify what applicant's invention is (see MPEP § 608.02g).

Correction is required.

Applicant is required to submit a proposed drawing correction, showing changes in red ink, in response to this Office action. However, formal correction of the noted defect(s) can be deferred until the application is allowed by the examiner (see MPEP § 608.02v).

Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 5-10 are rejected under 35 U. S. C. § 102 (b) as being anticipated by U.S. Patent No. 6,339,239 to Alsmeier et al.

Regarding to claim 1, Alsmeier discloses a memory device having a plurality of memory cells, wherein each memory cell comprises a trench capacitor (fig. 6) formed in a semiconductor substrate (col. 3, line 23) and an access transistor (col. 4, lines 17-37, figs. 4, 6) for it, wherein each access transistor comprises a first contact region 107 connected to an internal electrode of the trench capacitor, a second contact region 112 connected to a bit line and a control electrode region 102, wherein the control electrode regions of neighboring access transistors are connected by a word line 110/111 formed in the semiconductor substrate (col. 5, lines 14-31, and fig. 6).

Regarding to claim 2, the memory device wherein the trench capacitor is formed in a trench in the semiconductor substrate, wherein the semiconductor substrat

comprises a first region of a first conductivity type and an underlying second implanted region of a second conductivity type, wherein the trench of the memory cell extends over the first and second regions (fig. 6).

Regarding to claim 3, the memory device, wherein the access transistor is a field effect transistor having a channel region, wherein the control electrode region of the access transistor has an oxide layer separating the channel region of the access transistor from the control electrode region (col. 4, lines 17-37, figs. 4, 6).

Regarding to claim 5, the memory device wherein the control electrode oxide layer comprises an SiO.sub.2 material (col. 4, lines 17-37, figs 4, 6).

Regarding to claim 6, the memory device wherein the access transistor is a vertical field effect transistor (col. 5, lines 26-27, fig. 6).

Regarding to claim 7, the memory device wherein the channel region of the vertical field effect transistor is formed in the trench of the memory cell (figs. 4, 6).

Regarding to claim 8, the memory device wherein the control electrode region completely surrounds the channel region of the access transistor (figs. 4, 6).

Regarding to claim 9, the memory device wherein the access transistor is a tunnel transistor (figs. 4, 6).

Regarding to claim 10, the memory device wherein the word line is a highly doped region buried in the semiconductor substrate (figs. 4, 6).

Regarding to claim 12, the memory device, wherein the highly doped word line region is connected to the control electrode region of the access transistor.

Regarding to claim 13, the device wherein the first region, the second underlying region and the highly doped word line region are formed by means of implantation in the semiconductor substrate (figs. 4, 6).

Regarding to claim 14, the memory device wherein the highly doped word line region can be contacted outside the memory cell (figs. 4, 6).

Regarding to claim 15, the memory device wherein a plurality of memory cells can be combined to a memory cell field (figs. 4, 6).

Claim Rejections - 35 U.S.C. § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4, 11, 16, and 17 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,339,239 to Alsmeier et al. in view of the remark.

Regarding to claim 4, Alsmeier discloses the claimed invention except for the memory device wherein the layer thickness of the control electrode oxide layer is in a range of 0.5 to 15 nm and is preferably in a range of 3 to 6 nm.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the layer thickness of the control electrode oxide layer is in a range of 0.5 to 15 nm and is preferably in a range of 3 to 6 nm, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding to claim 11, Alsmeier discloses the claimed invention except for the memory device, wherein the word line is a highly doped region of the second conductivity type completely formed in the first region of the semiconductor substrate and surrounded by it, and is isolated from the second region by the first region.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the word line is a highly doped region of the second conductivity type completely formed in the first region of the semiconductor substrate and surrounded by it, and is isolated from the second region by the first region.

Regarding to claim 16, Alsmeier discloses the claimed invention except for the memory device wherein the first conductivity type is a p conductivity type and the second conductivity type is an n conductivity type.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the first conductivity type is a p conductivity type and the second conductivity type is an n conductivity type.

Regarding to claim 17, Alsmeier discloses the claimed invention except for the memory device wherein the first conductivity type is an n conductivity type and the second conductivity type is a p conductivity type.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the first conductivity type is an n conductivity type and the second conductivity type is a p conductivity type.

Conclusion

Any inquiry concerning this communication on earlier communications from the examiner should be directed to Mai-Huong Tran, (571) 272-1796. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 6:30 PM. The examiner's supervisor, David Nelms can be reached on (571) 272-1787.

The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR, Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mai-Huong Tran